High-Efficiency High-Level Modulator for Use in Dynamic Envelope Tracking CDMA RF Power Amplifiers

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***Abstract* — There is an inherent tradeoff between linearity and efficiency in modern microwave power amplifiers using spectrally efficient modulation techniques. This paper discusses an envelope modulation technique to improve efficiency while preserving linearity when modulating the supply voltage to the PA. Based on the SEPIC (Single-Ended Primary Inductance Converter) switchmode topology with coupled inductors, a continuous current mode (CCM) converter is used as a high-level class-S supply modulator to track the carrier envelope of a CDMA transmit signal. This results in a considerable improvement in PA efficiency while preserving linearity and modulation accuracy. Modulation frequencies up to 1.25 MHz are reproduced with about 80% efficiency. A SPICE compatible switched average converter model is described with an expression for an average current mode (ACM) control duty cycle generator. Simulated and measured data are presented for the case of a LDMOS class-AB RF amplifier with a SEPIC class-S modulated supply under IS-95 CDMA signal drive conditions.**

I. Introduction

Spectral regrowth must be limited to prevent adjacent channel splatter in cellular systems employing digital modulation schemes such as CDMA. This requires a very high degree of linearity from the RF power amplifiers. Typically, these PAs are operated in Class A or Class AB mode in base station applications, and require the use of feedforward techniques. Power control is usually needed over a wide dynamic range, so it is common for a high-power transmitter to operate at low power levels for a large percentage of time. Linearly-biased PA efficiency can be quite poor under these circumstances, on the order of one-percent. This has a direct impact on cost, size, and thermal management. Over the years, a number of alternative designs have been proposed to circumvent the inherent tradeoff between linearity and efficiency. For example, LINC (LInear amplification using Non-linear Circuits) [1], Kahn EER (Envelope Elimination & Restoration) [2]-[4], dynamic carrier envelope tracking [5], [6] and other techniques [7], [8] have been addressed in recent papers.

II. Envelope Tracking Signal Characteristics

The carrier envelope tracking technique has the advantage of preserving the amplitude and phase information of the RF carrier when it is (typically) operating at very low power levels. A slight improvement in efficiency is sacrificed to preserve modulation accuracy at low power, but this occurs when the power dissipated is minimal. The modulating waveform used for envelope tracking can be chosen to enhance amplifier efficiency, and at the same time preserve the gain-linearity of the device, while minimizing the required supply modulation bandwidth. Other benefits include limiting the PA's minimum operating voltage for very low or zero envelope input, e.g., WCDMA or multi-carrier operation. This reduces the dynamic range requirement of the modulator and improves the stability of the RF device.

In CDMA base station applications, RF stages are used to amplify transmit signals that can be represented by

$$S(t) = \mathrm{Re}\left[R(t) e^{j\omega t} \right] \tag{1}$$

where

$$R(t) = \sum_k g(t - kT_c)\cos(\Phi_k) + j\sum_k g(t - kT_c)\sin(\Phi_k). \tag{2}$$

In this normalized expression g(t) is the unit impulse response of the cascaded transmitter filter and phase equalizer as defined in IS-95. $\Phi_k(t)$ is the phase of the k^{th} chip occurring at discrete time $t_k = T_c$ where T_c is the chip duration. To preserve the linearity of LDMOS power FETs operating under class AB service, the supply voltage envelope tracking function

$$V(t) = m + nR(t)R^*(t) = m + \hat{n}\left(I^2(t) + Q^2(t)\right) \tag{3}$$

can be employed to provide a significant improvement in drain efficiency. The quantity 'm' is chosen to be greater than the minimum supply voltage. For IS-95, the envelope tracking function's bandwidth is equal to the passband channel bandwidth (1.23 MHz).

Using (3), the supply voltage mapping of gain versus output power for a Motorola PFP9045 LDMOS FET is shown in Fig. 1.

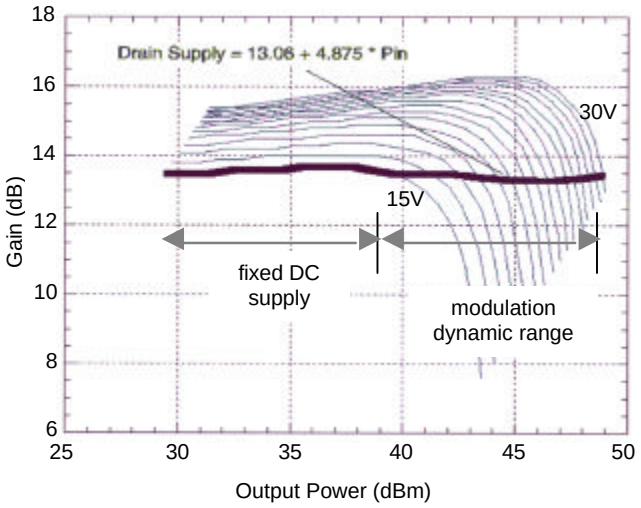

Fig. 1. Measured gain versus output power for LDMOS device at various values of drain supply from 15 to 30 Vdc.

III. Converter Characteristics

A DC-AC inverter with rectifier is employed as a Class-S modulator to act as an ideal voltage source and deliver the desired supply voltage as shown in Fig. 2.

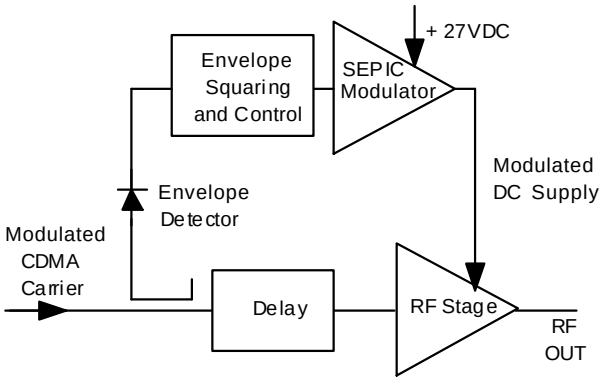

Fig. 2. Block diagram of SEPIC and RF stage.

To meet the low source impedance requirement, CCM operation is preferred. Non-inverting buck/boost operation is desirable when operating with a variable DC supply input; therefore, the non-isolated SEPIC converter topology (Fig. 3) can be used. This circuit has the important advantage that it can employ a grounded-source N-channel FET for EMI-suppression. The gate drive is ground-referenced rather than floating. The SEPIC's DC-DC non-linear voltage transfer function is given by $D/(1-D)$ as shown in Fig. 4. This circuit has been operated successfully at a square-wave switching frequency of 20 MHz and a control voltage duty cycle, D, as high as 0.6.

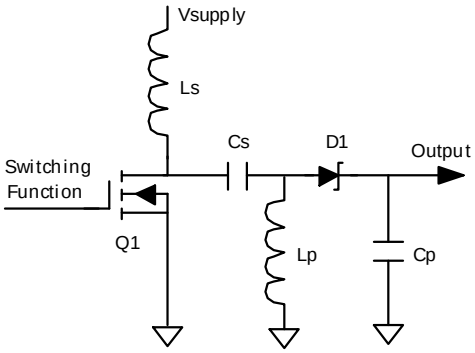

Fig. 3. SEPIC switching cell schematic diagram.

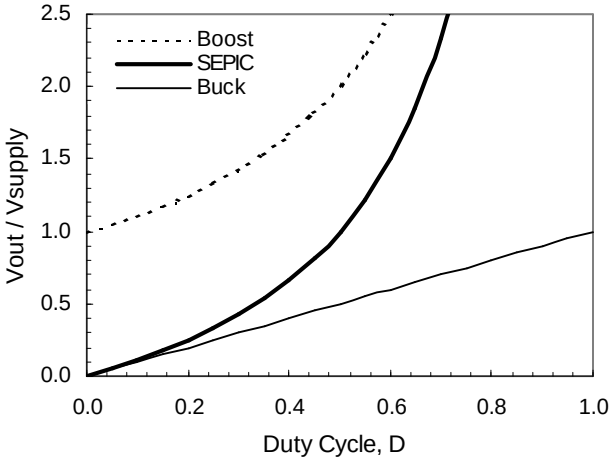

Fig. 4. Modulator voltage gain versus duty cycle, D.

A voltage feedback loop and two current feedback loops are used to control the SEPIC switching cell as shown in Fig. 5. One current loop provides a low-frequency path and the other provides a high-frequency path. Inductors *Lp*, *Ls* and *Lx* are coupled magnetically to achieve extended operating bandwidth and improved average current mode control. This moves a RHP zero to a higher frequency in the small signal (control to output) transfer function. The high-frequency path provides high-frequency current feedback without excess phase shift. The result is an increase in control loop phase margin, greater large-signal dynamic range, and an improvement in linearity.

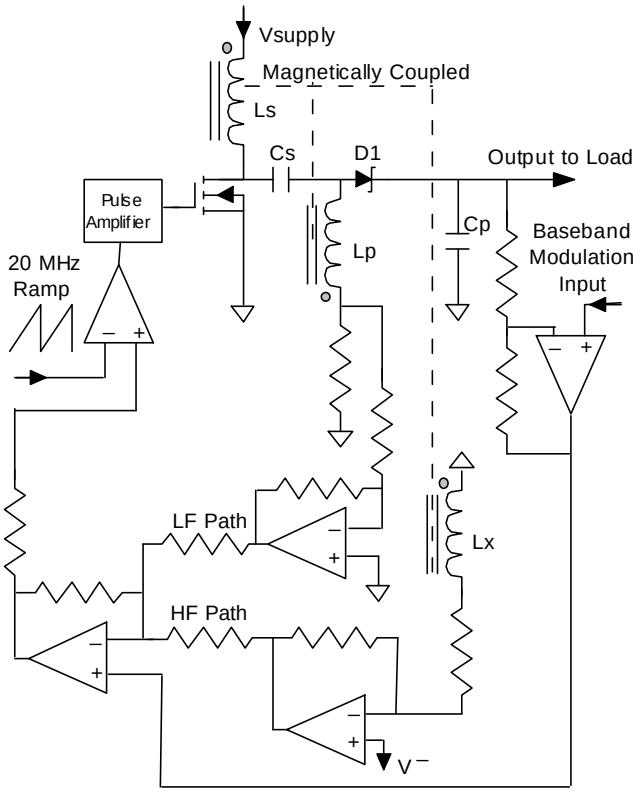

Fig. 5. Detailed SEPIC control loop with coupled inductors.

IV. Behavioral Average Model

The average model of the SEPIC modulator is shown in Fig. 6. It is based on the Switched Inductor Model [9], [10]. Average current mode control is modeled with a 'Duty Cycle Generator' [9] to represent the relationship between the modulation input and the average duty cycle behavior of the converter. For this circuit, the average control voltage D_{on} is given by the implicit relationship

$$D_{on} = D_{on}\left(1 + M_s T_s/2\right) - V_{acm} + \left(D_{on} - 1\right) D_{on}\left(T_s/2\right)\left|K_s\left(V_{cs} - V_{sw(on)}\right)/L_m\right| + \left(1 - D_{on}\right)^2\left(T_s/2\right)\left|K_s\left(V_{diode} + V_{cp}\right)/L_m\right| \quad (4)$$

where D_{on} is the average control voltage per switching cycle in V, M_s is the slope compensation constant in V/s, T_s is the switching period, V_{acm} is the error voltage of combined current and voltage feedback loops, K_s is the sensed current conversion gain in V/A, V_{cs} is the voltage across C_s, $V_{sw(on)}$ is the 'on'-voltage across the switching device, L_m is the mutual coupling inductance, V_{diode} is the voltage drop across the Schottky diode *D1*, and V_{cp} is the voltage across C_p.

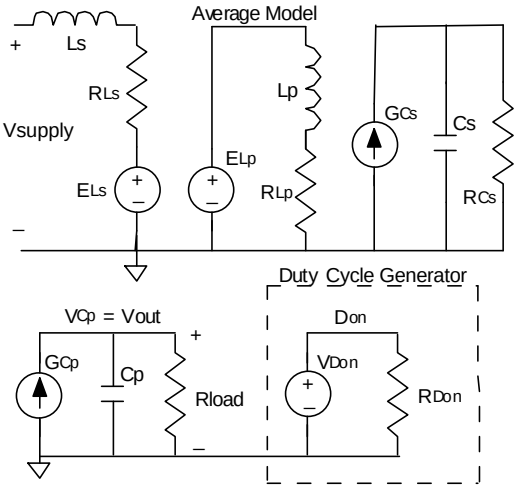

Fig. 6. SEPIC average model.

It is possible to derive an *explicit*, albeit complicated, expression for D_{on} as a function of the other parameters. From a CAD modeling standpoint using PSPICE or ADS, the implicit form shown in (4) is more convenient.

V. Modulator Performance

The SEPIC modulator (Fig. 7.) was configured to deliver 125 watts into a five-ohm resistive load where the measured efficiency was 80%. A plot of open- and closed-loop transfer gain performance is shown in Figs. 8 and 9.

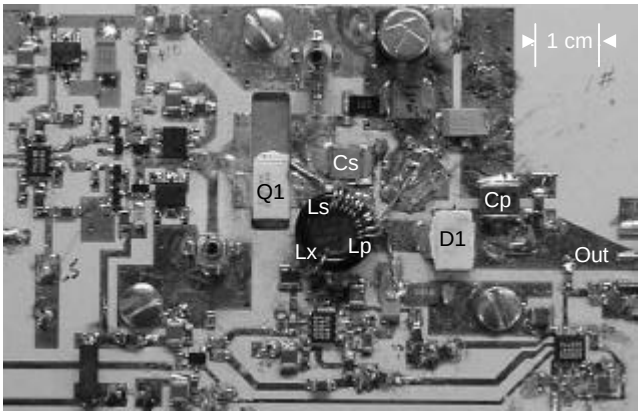

Fig. 7. Photograph of SEPIC-based modulator.

A Motorola MRF9045 45W LDMOS PA stage was driven at 881.5 MHz with an IS-95 CDMA signal (9 traffic channels + pilot/paging/sync). The SEPIC-based circuit (Fig. 5) was used to modulate the supply to the

Class AB RF stage. The change in spectral regrowth was not significant in the adjacent channel region (± 1.25 MHz). Fig. 10 shows the resulting adjacent channel power of the output spectrum. The measured drain efficiency of the LDMOS stage improved from 20% to 32% under these operating conditions.

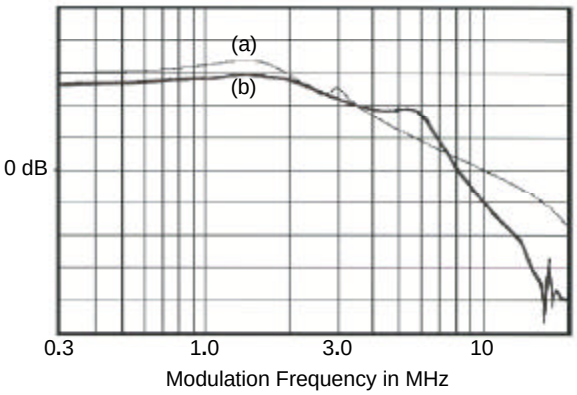

Fig. 8. Open-loop magnitude response versus frequency of modulator: (a) simulated, (b) measured. Vert: 10 dB/div.

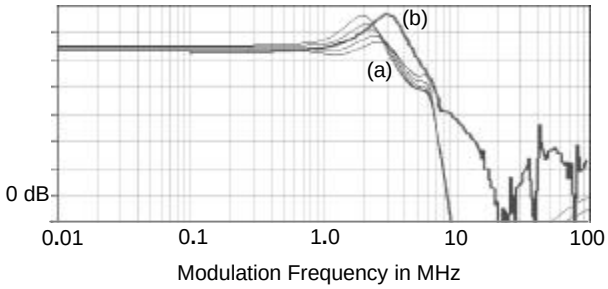

Fig. 9. Closed-loop magnitude response versus frequency of modulator: (a) simulated, (b) measured. Vert: 5 dB/div.

VI. Summary

A new SEPIC topology has been simulated, built and tested with a square-wave switching frequency of 20 MHz and a closed-loop modulation bandwidth of 1.25 MHz. An expression (4) and an average model (Fig. 6) have been derived to simulate the closed-loop performance of the modulator. The efficiency of the SEPIC modulator was measured to be 80%. When used to modulate the DC supply to an RF stage, the overall efficiency was increased from 20% to 32% for a CDMA IS-95 transmit signal.

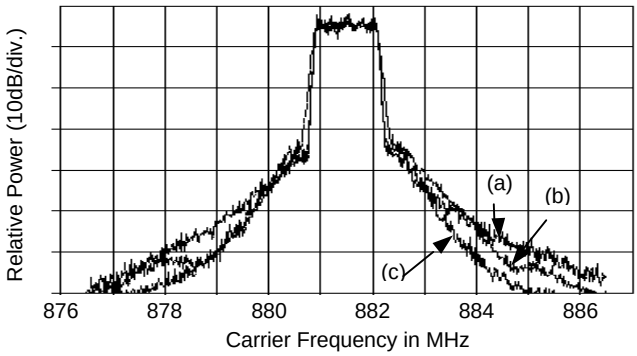

Fig. 10. CDMA spectrum of RF amplifier at 10W output power. (a) modulator with delay matching, (b) modulator without delay matching, (c) fixed supply voltage without modulation.

References

[1] B. Stengel and W. R. Eisenstadt, "LINC power amplifier combiner method efficiency optimization," *IEEE Trans. Vehicular Tech.*, Vol. 49, No. 1, pp. 229-234, Jan. 2000.

[2] F. H. Raab and D. J. Rupp, "Class-S High-Efficiency Amplitude Modulator," *RF Design*, pp. 70-74, May 1994.

[3] F. H. Raab, "Intermodulation Distortion in Kahn-Technique Transmitters," *IEEE Trans. Microwave Theory & Tech.*, Vol. MTT-44, No. 12, pp. 2273-2278, Dec. 1996.

[4] F. H. Raab, B. E. Sigmon, R. G. Myers, and R. M. Jackson, "L-Band Transmitter Using Kahn EER Technique," *IEEE Trans. Microwave Theory & Tech.*, Vol. 46, No. 12, pp. 2220-2225, Dec. 1998.

[5] G. Hanington, P. Chen, P. Asbeck, and L. Larson, "High-Efficiency Power Amplifier Using Dynamic Power-Supply Voltage for CDMA Applications," *IEEE Trans. Microwave Theory & Tech.*, Vol. 47, No. 8, pp. 1471-1476, Aug. 1999.

[6] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R. Sherman, and T. Quach, "High efficiency CDMA RF power amplifier using dynamic envelope tracking technique," *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, WE3A-6, vol. 2, pp. 873-876, June 2000.

[7] A. Jayaraman, P. F. Chen, G. Hanington, L. Larson, and P. Asbeck, "Linear High-Efficiency Microwave Power Amplifiers Using Bandpass Delta-Sigma Modulators," *IEEE Microwave and Guided Wave Letters*, Vol. 8, No. 3, pp. 121-123, March 1998.

[8] T. B. Mader, E. W. Bryerton, M. Markovic, M. Forman, and Z. Popovic, "Switched-Mode High-Efficiency Microwave Power Amplifiers in a Free-Space Power-Combiner Array," *IEEE Trans. Microwave Theory & Tech.*, Vol. 46, No. 10, pp. 1391-1398, Oct. 1998.

[9] S. Ben-Yaakov, D. Adar, and G. Rahav, "A SPICE Compatible Behavioral Model of SEPIC Converters," *1996 IEEE 27th Power Electronics. Specialists Conf.*, Vol. 2, pp. 1668-1674, June 1996.

[10] D. Adar, G. Rahav and S. Ben-Yaakov, "A unified behavioral average model of SEPIC converters with coupled inductors," *1997 IEEE 28th Power Electronics. Specialists Conf.*, Vol. 1, pp. 441-446, June 1997.